

REMARK

Applicants respectfully request reconsideration of this application as amended. Claims 46, 48, 54-55, 59, 61, and 67 have been amended. No claims have been cancelled or added. Therefore, claims 46-67 are now presented for examination.

Claim Rejections under 35 U.S.C. § 112

Claim 59 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 59 has been amended to insert the word “the” before “semiconductor device”. In addition, to correct the grammar of this claim “equalize” has been changed to “equalizes”.

Applicant respectfully submits that the rejection has been fully met, and requests that the rejection be withdrawn.

Claim Rejection under 35 U.S.C. §102

Choi

The Examiner rejected claims 46, 48-55 and 57-60 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,959,919 of Choi (“Choi”).

As amended herein, Claim 46 reads as follows:

46. A method comprising:
receiving a signal pulse; and
in response to the signal pulse:

pulling a voltage of a sense input node for a non-volatile memory cell to a voltage potential of a voltage source;
pulling a voltage of a reference input node for a reference cell to the voltage potential of the voltage source;
and
shorting a sense node for the non-volatile memory cell to a reference node for the reference cell.

Among other provisions, the claim provides that a voltage of a sense input node for a memory cell and a voltage of a reference input node for a reference cell are pulled to a voltage potential of a voltage source. As shown, for example, in Figure 6 of the application, the introduction of a signal (kicker enable 650) provides a path from voltage source V_{CC} 660 to either the SIN node or the RIN node 640.

With regard to this element of the claim the Office Action cites to Figure 2 of Choi. In Figure 2, an equalization signal EQ is applied. The inverse signal /EQ may be applied to pre-charging part 25, specifically to PMOS transistor MP21 in first pre-charging means 25-1 and to PMOS transistor MP24 in second pre-charging means 25-2.

Among other differences between claim 46 and Choi, it is clear that the input node for the dummy cell (being applied to transistor MN21 in sense amplifier 26) and the input node for the memory cell (being applied to transistor MN22 in sense amplifier 26) are *not* pulled to the voltage of the voltage source when signal EQ is applied. The existence of diode-connected transistor MP22 between MP21 and the input node for the dummy cell and diode-connected transistor MP25 between MP24 and the input node for the memory cell make it clear that the voltages of the relevant nodes will be less than the

voltage of the voltage source. As the system is described in Choi, there is no possibility or intention of pulling the input voltages to the voltage of the voltage source.

For at least the above reasons, it is respectfully submitted that Choi does not anticipate the provisions of Claim 46. It is submitted that the above arguments also apply to independent claim 55, and thus such claim also is not anticipated by Choi. The remaining claims are claims dependent on claims 46 and 55 and thus are allowable as being dependent on the allowable base claims.

Claim Rejection under 35 U.S.C. §102

Yero

The Examiner rejected claims 47, 56 and 61-67 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,038,173 of Yero ("Yero").

In addition to any other differences between Yero and the claims herein, Yero suffers from the same deficiency as that described above with regard to Choi. Yero does not provide for pulling a sense input node and a reference input node to a voltage of a voltage source.

The pre-charging process of Yero is described from column 4, line 46 through column 5, line 7. It is clear from this description that Yero does not pull the sense input node and the reference input node to the voltage of the voltage source. In the system described in Yero and shown in Figures 2 and 3, when the pre-charging potential of the LB (bit line) and the LR (reference line) reach one volt, the NAND gate goes to a high level, thereby interrupted the pre-charging process. With the pre-charging process halting at one volt, the voltages of the relevant nodes will not reach the potential of the voltage

source. As with Choi, there is no possibility or intention of pulling the lines to the voltage potential of the voltage source.

Based on the above arguments, independent Claims 61 and 67, as well as Claims 46 and 55, are not anticipated by Yero. Rejected Claims 47 and 56 are dependent on Claims 46 and 55 respectively and thus are allowable as being dependent on the allowable base claims. Claims 62-66 are dependent on claim 61 and thus are allowable because they are dependent on an allowable base claim.

Conclusion

Applicant respectfully submits that the rejections have been overcome by the amendment and remark, and that the claims as amended are now in condition for allowance. Accordingly, Applicant respectfully requests the rejections be withdrawn and the claims as amended be allowed.

Invitation for a Telephone Interview

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Request for an Extension of Time

Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

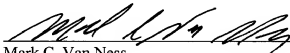
Charge our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 4/15/03



Mark C. Van Ness
Reg. No. 39,865

12400 Wilshire Boulevard
7th Floor
Los Angeles, California 90025-1030
(303) 740-1980